LH521028A

CMOS 64K × 18 Static RAM

FEATURES

- Fast Access Times: 15/17/20/25/35 ns
- Wide Word (18-Bits) for:
  – Improved Performance
  – Reduced Component Count
  – Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low-Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention
- JEDEC Standard Pinout
- Package: 52-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH521028 is a high-speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable ($\overline{W}$), Chip Enable ($\overline{E}$), High and Low Byte Select ($\overline{S}_L$ and $\overline{S}_H$), Output Enable ($\overline{G}$) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH).The Byte-select controls, $\overline{S}_H$ and $\overline{S}_L$, are also used to enable or disable Read and Write operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Address bus buffers and/or latches.

Write cycles occur when Chip Enable ($\overline{E}$), $\overline{S}_H$ and/or $\overline{S}_L$, and Write Enable ($\overline{W}$) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ and either $\overline{S}_H$ or $\overline{S}_L$ are LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

PIN CONNECTIONS

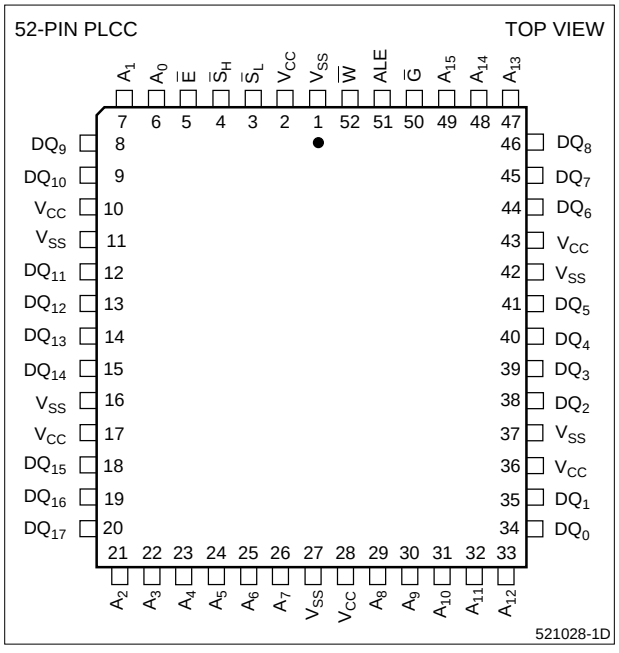


Figure 1. Pin Connections for PLCC Package

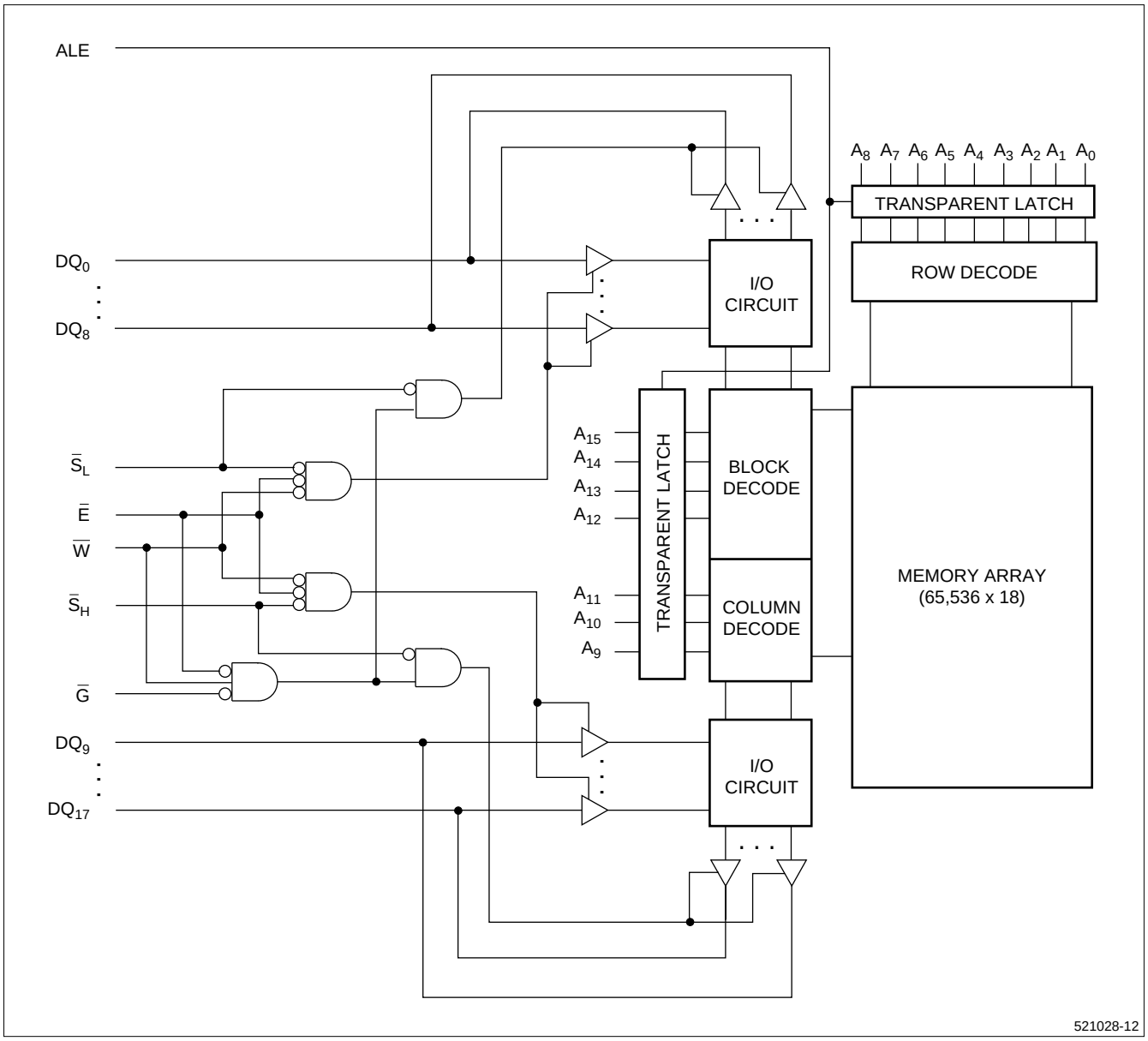


Figure 2. LH521028A Block Diagram

TRUTH TABLE

ADDRESS	$\overline{E}$	$\overline{S}_H$	$\overline{S}_L$	ALE	$\overline{G}$	$\overline{W}$	DQ_0-DQ_8	DQ_9-DQ_{17}	MODE	I_{CC}
Don't Care	H	X	X	H	X	X	High-Z	High-Z	Standby	I_{SB}
Valid	L	L	H	H	L	H	Active	High-Z	Read	I_{CC1}
Valid	L	H	L	H	L	H	High-Z	Active	Read	I_{CC1}
Valid	L	L	L	H	L	H	Active	Active	Read	I_{CC1}
Valid	L	L	L	H	H	H	High-Z	High-Z	Read	I_{CC1}
Don't Care	L	L	L	L	L	H	Data Out	Data Out	Read	I_{CC1}
Valid	L	L	H	H	X	L	Data In	Don't Care	Write, low byte	I_{CC1}
Valid	L	H	L	H	X	L	Don't Care	Data In	Write, high byte	I_{CC1}
Valid	L	L	L	H	X	L	Data In	Data In	Write, both bytes	I_{CC1}
Valid	L	H	H	H	X	L	Don't Care	Don't Care	Write, inhibited	I_{CC1}
Don't Care	L	L	L	L	X	L	Data In	Data In	Write, both bytes	I_{CC1}

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	SIGNAL
1	V_{SS}
2	V_{CC}
3	$\overline{S}_L$
4	$\overline{S}_H$
5	$\overline{E}$
6	A_0
7	A_1
8	DQ_9
9	DQ_{10}
10	V_{CC}
11	V_{SS}
12	DQ_{11}
13	DQ_{12}

PIN	SIGNAL
14	DQ_{13}
15	DQ_{14}
16	V_{SS}
17	V_{CC}
18	DQ_{15}
19	DQ_{16}
20	DQ_{17}
21	A_2
22	A_3
23	A_4
24	A_5
25	A_6
26	A_7

PIN	SIGNAL
27	V_{SS}
28	V_{CC}
29	A_8
30	A_9
31	A_{10}
32	A_{11}
33	A_{12}
34	DQ_0
35	DQ_1
36	V_{CC}
37	V_{SS}
38	DQ_2
39	DQ_3

PIN	SIGNAL
40	DQ_4
41	DQ_5
42	V_{SS}
43	V_{CC}
44	DQ_6
45	DQ_7
46	DQ_8
47	A_{13}
48	A_{14}
49	A_{15}
50	$\overline{G}$
51	ALE
52	$\overline{W}$

PIN DEFINITIONS

V_{CC} Positive Supply Voltage Terminals

V_{SS} Reference Terminals

$A_0 – A_{15}$ Address Bus Input

The Address bus is decoded to select one 18-bit word out of the total 64K words for Read and Write operations.

$\overline{E}$ Chip Enable Active LOW Input

Chip Enable is used to enable the device for Read and Write operations. When HIGH, both Read and Write operations are disabled and the device is in a reduced power state. When LOW, a Read or Write operation is enabled.

$\overline{W}$ Write Enable Active LOW Input

Write Enable is used to select either Read or Write operations when the device is enabled. When Write Enable is HIGH and the device is Enabled, a Read operation is selected. When Write Enable is LOW and the device is enabled, a Write operation is selected. A Byte-write operation is available by using the Byte-select controls.

$\overline{S}_H$, $\overline{S}_L$ Select High Select Low Active LOW Inputs

The Select High and Select Low signals, in conjunction with the Chip Enable and Write Enable signals, allow the selection of the individual bytes for Read and Write operations. When High, the Select signal will deselect its byte and prevent Read or Write operations. When the Select signal is LOW and Chip Enable is LOW, a Read or Write operation is performed at the location determined by the contents of the Address bus. When Chip Enable is HIGH, the Select signals are Don't Care. Select Low ($\overline{S}_L$) is assigned to $DQ_0 – DQ_8$ and Select High ($\overline{S}_H$) is assigned to $DQ_9 – DQ_{17}$.

ALE Address Latch Enable Active High Input

The Address Latch Enable signal is used to control the Transparent latches on the Address bus. The Latches are transparent when HIGH and are latched when LOW. If not required, Address Latch Enable may be tied HIGH, leaving the Address bus in a transparent condition.

$DQ_0 – DQ_{17}$ Data Bus Input/Output

$DQ_0 – DQ_8$ comprise the Low byte, selected by $\overline{S}_L$, and $DQ_9 – DQ_{17}$ comprise the High Data byte, selected by $\overline{S}_H$. The Data Bus is in a high impedance input mode during Write operations and standby. The Data bus is in a low-impedance output mode during Read operations.

$\overline{G}$ Output Enable Active LOW Input

The Output Enable signal is used to control the output buffers on the Data Input/Output bus. When $\overline{G}$ is HIGH, all output buffers are forced to a high impedance condition. When $\overline{G}$ is LOW, the output buffers will become active only during a Read operation ($\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ are LOW, $\overline{W}$ is HIGH).

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	–0.5 V to 7 V
Input Voltage Range	–0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Package Limit)	2 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	–0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = minimum			300	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V f = 0			4	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}			50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	–2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	–2		2	µA
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

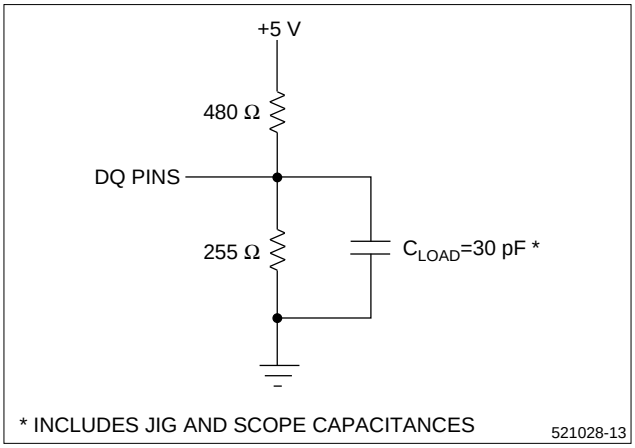


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{DQ} (I/O Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	–15		–17		–20		–25		–35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE												
t_{RC}	Read Cycle Timing	15		17		20		25		35		ns
t_{AA}	Address Access Time		15		17		20		25		35	ns
t_{ASL}	Address Setup to Latch Enable	2		2		2		2		2		ns
t_{AHL}	Address Hold from Latch Enable	3		3		4		4		4		ns
t_{LEA}	Latch Enable to Data Valid		16		18		21		26		36	ns
t_{LHM}	Latch Enable High Pulse Width	5		5		5		5		5		ns
t_{OH}	Output Hold from Address Change	4		4		4		4		4		ns
t_{LH}	Output Hold from Latch High	4.5		4.5		4.5		4.5		4.5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		15		17		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		9		10		10		12		20	ns
t_{SA}	$\overline{S}$ Low to Valid Data		7		8		10		12		20	ns
t_{SLZ}	$\overline{S}$ Low to Output Active [2,3]	2		2		2		3		3		ns
t_{SHZ}	$\overline{S}$ High to Output High-Z [2,3]		10		10		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		7		8		9		12		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		7		8		8		10		20	ns
t_{RCS}	Read Setup from $\overline{W}$ High	0		0		0		0		0		ns
t_{RCH}	Read Hold from $\overline{W}$ Low	0		0		0		0		0		ns
t_{PU}	$\overline{E}$ LOW to Power Up Time [3]	0		0		0		0		0		ns
t_{PD}	$\overline{E}$ HIGH to Power Down Time [3]		15		17		20		25		35	ns
t_{WA}	Access Time From Write Enable HIGH		18		20		20		25		35	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15		17		20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	11		12		13		20		30		ns
t_{SW}	$\overline{S}$ LOW to End of Write	7		8		10		20		30		ns
t_{AW}	Address Valid to End of Write	11		12		13		20		30		ns
t_{AS}	Address Setup to Start of Write	0		0		0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		0		0		ns
t_{ASL}	Address Setup to Latch Enable	2		2		2		2		2		ns
t_{AHL}	Address Hold from Latch Enable	3		3		4		4		4		ns
t_{LHW}	Latch Hold from $\overline{W}$ High	0		0		0		0		0		ns
t_{LHM}	Latch Enable HIGH Pulse Width	5		5		5		5		5		ns
t_{WP}	$\overline{W}$ Pulse Width	11		12		13		20		30		ns
t_{DW}	Input Data Setup Time	7		8		9		10		15		ns
t_{DH}	Input Data Hold Time	0		0		0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		7		8		8		10		14	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1 (Unlatched Address Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode), $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following a $\overline{W}$-controlled Write cycle, t_{WA} and t_{AA} must both be satisfied to ensure valid data. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2 (Unlatched Chip Enable Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when $\overline{E}$, $\overline{S}$, and $\overline{G}$ are stable until the first address transition. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.

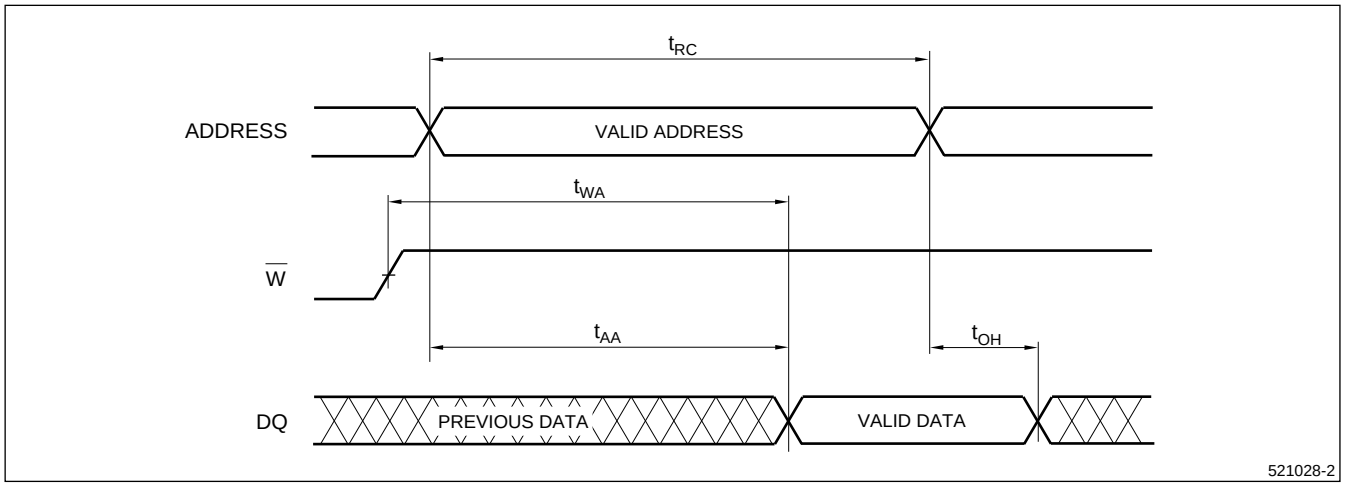


Figure 4. Read Cycle No. 1

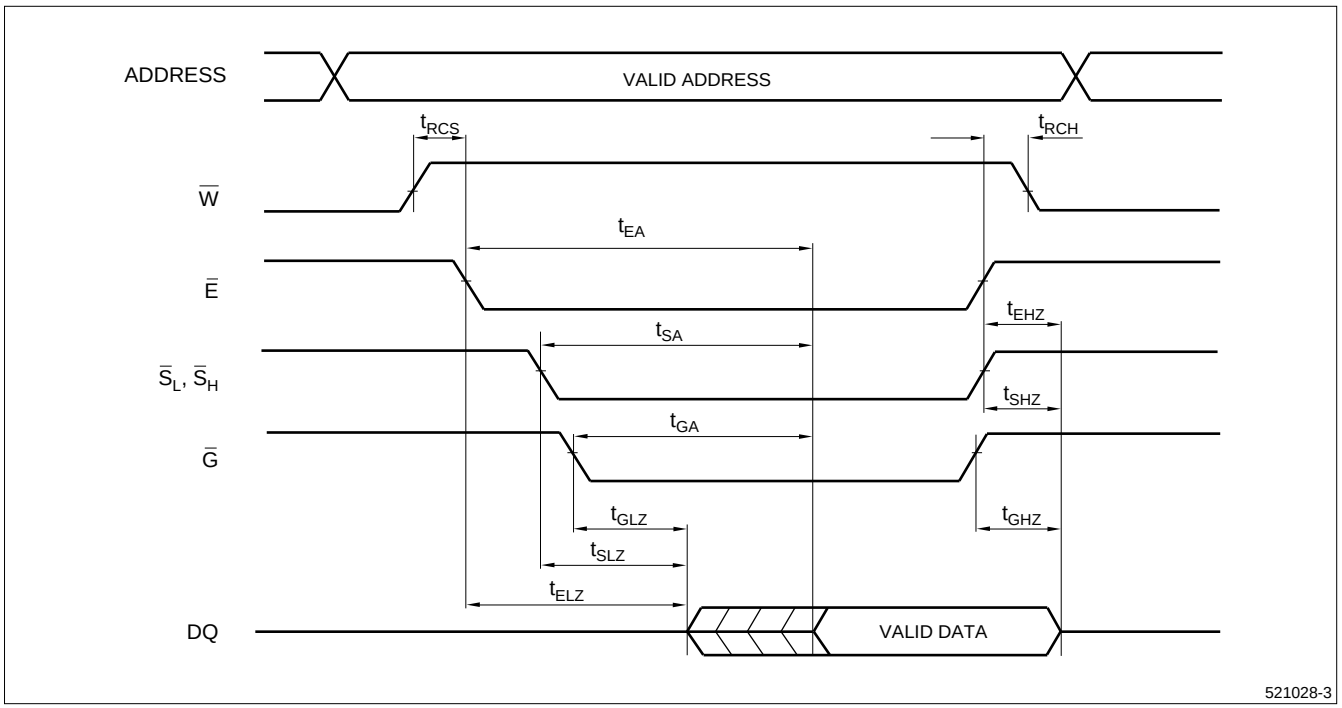


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 3
(Latched Address Controlled Read)

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$, $\overline{S}_H$, $\overline{S}_L$ and $\overline{G}$ are LOW. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of ALE, then the access time is t_{LEA}. If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA}. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

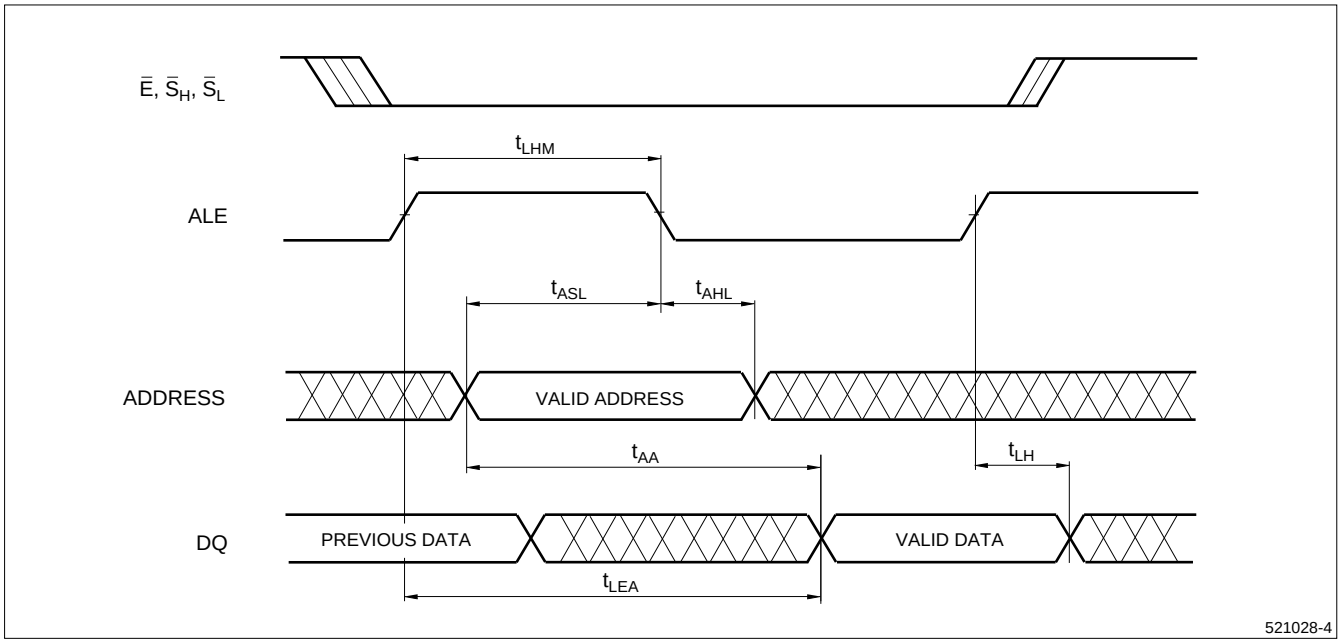


Figure 6. Read Cycle No. 3

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 4

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, t_{SA} and t_{GA}, but may become active as early as t_{ELZ}, t_{SLZ} or t_{GLZ}.

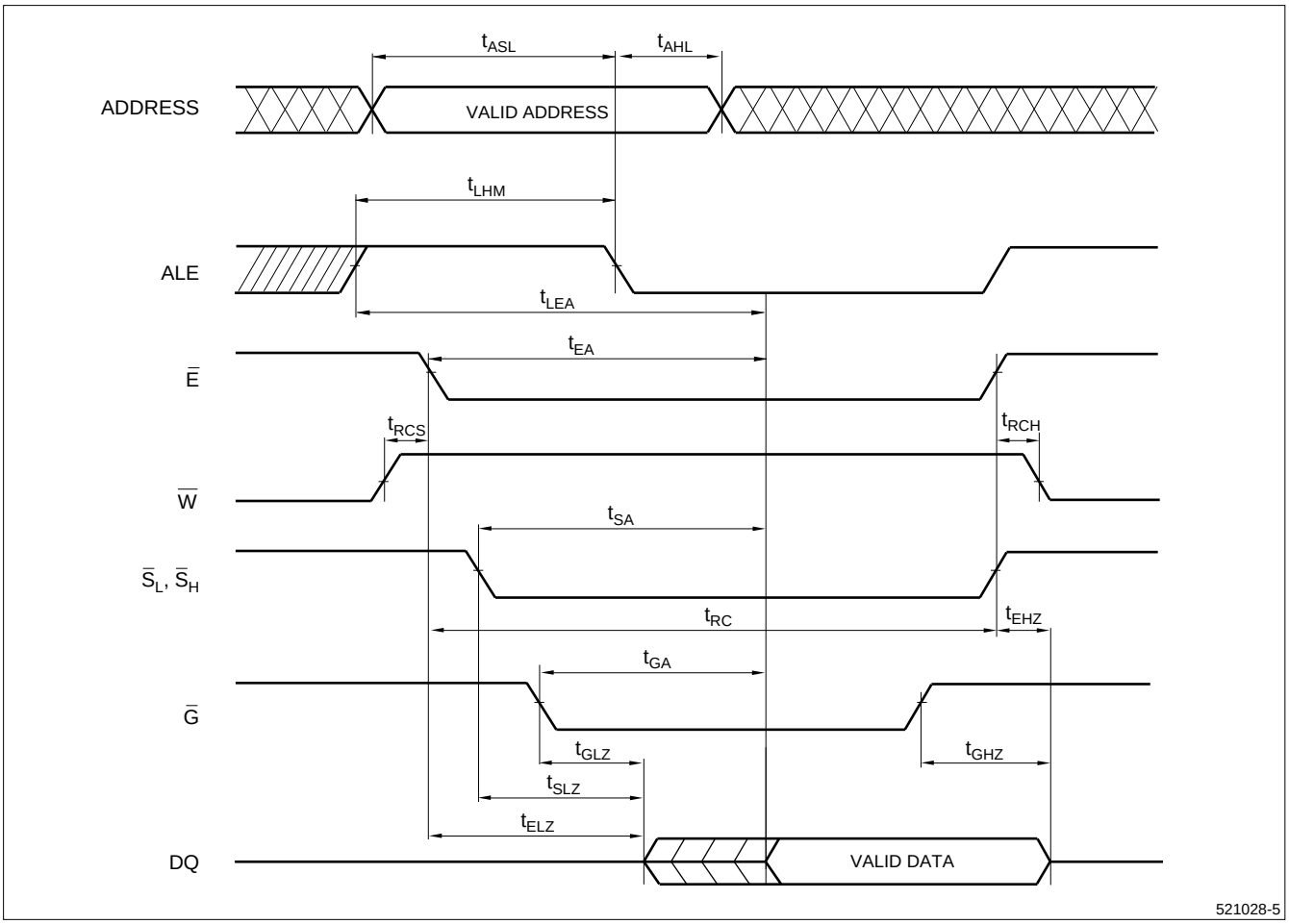


Figure 7. Read Cycle No. 4

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ go LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (Unlatched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW, ALE is High. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$, $\overline{S}_L$, $\overline{S}_H$ Controlled Write)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$, $\overline{S}_H$/$\overline{S}_L$ if $\overline{G}$ is LOW.

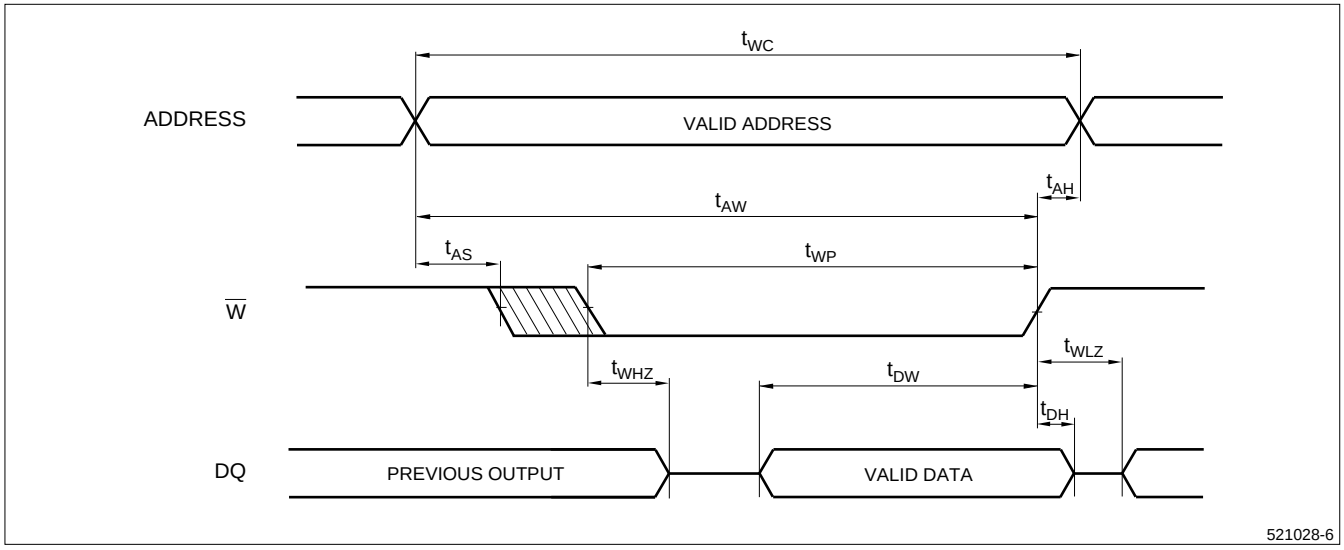


Figure 8. Write Cycle No. 1

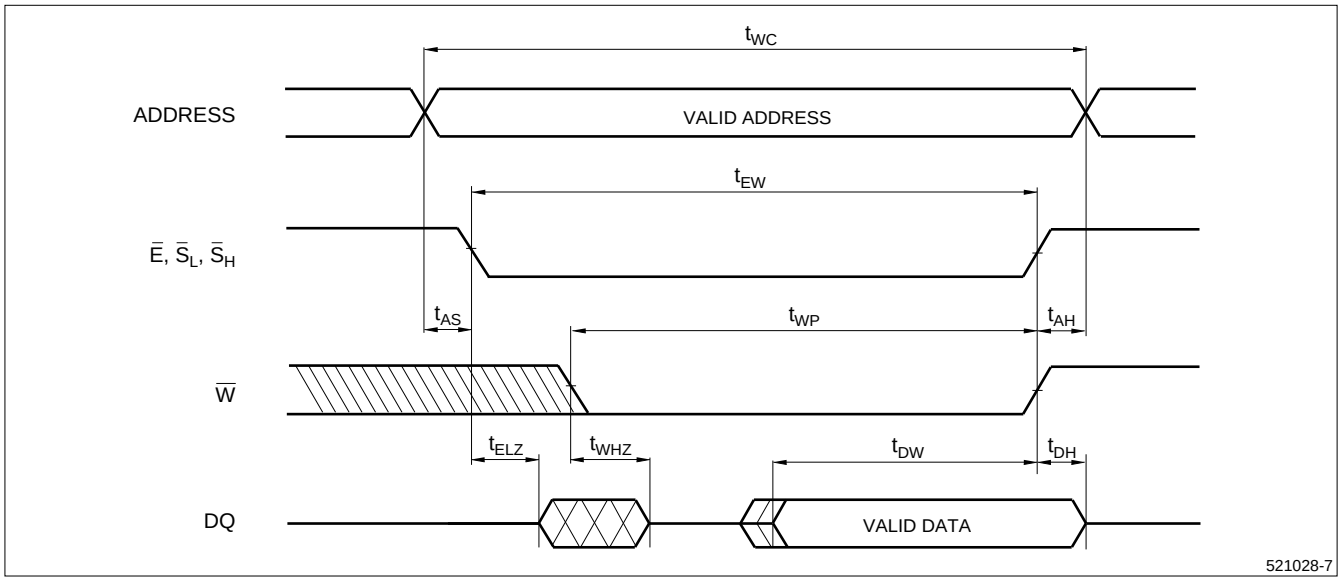


Figure 9. Write Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE (cont'd)

Write Cycle No. 3 (Latched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW.

Write Cycle No. 4 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edges of $\overline{E}$ and $\overline{S}_H$/$\overline{S}_L$.

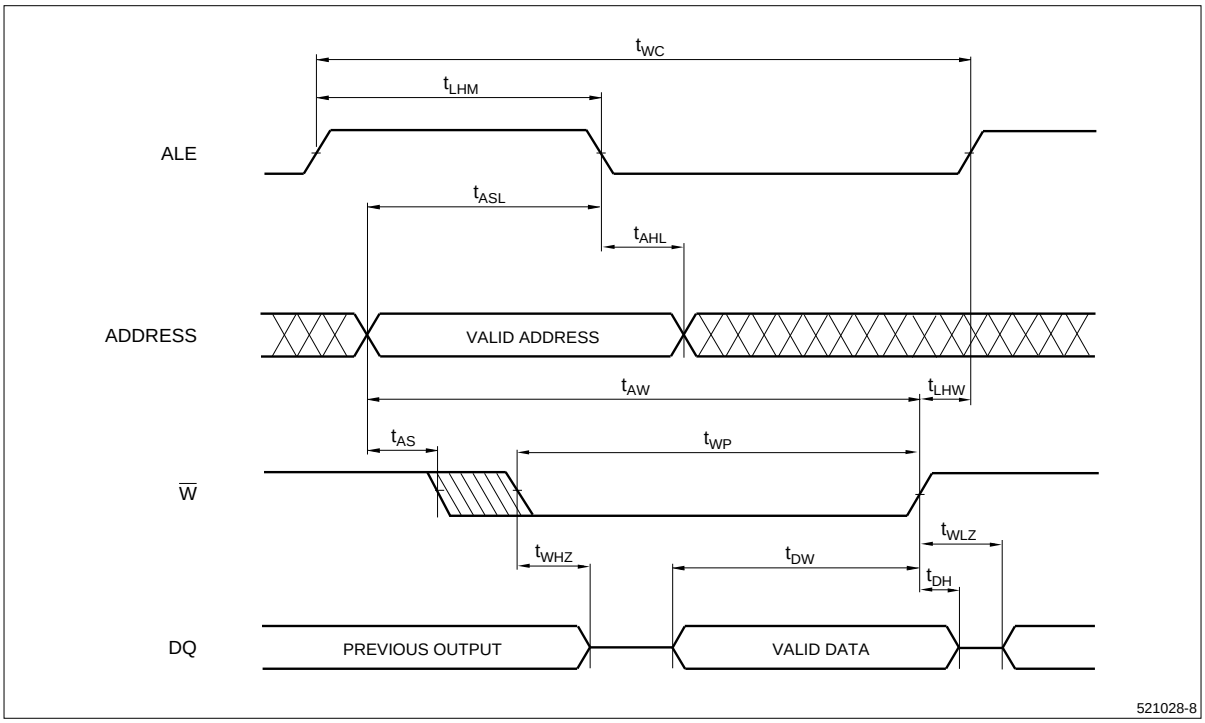


Figure 10. Write Cycle No. 3

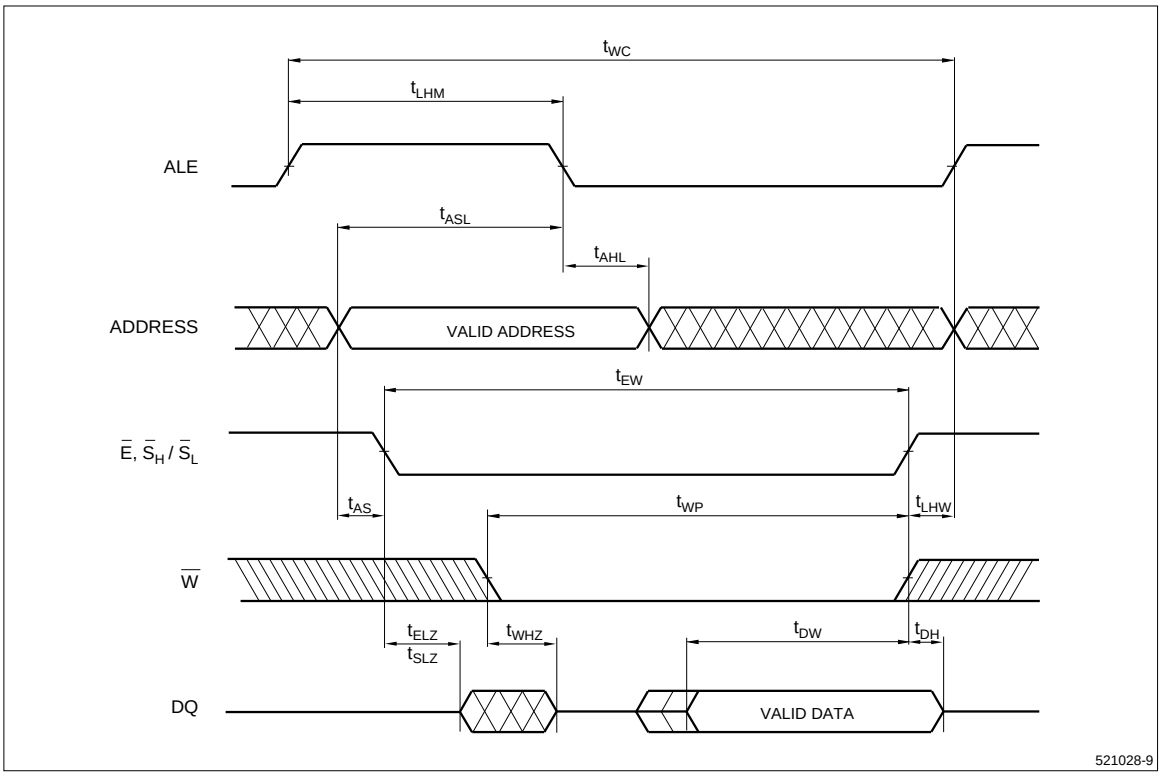


Figure 11. Write Cycle No. 4

BYTE OPERATIONS

Byte Read Description (Figure 12)

To read individual bytes, the device must be enabled ($\overline{E}$ is LOW), $\overline{W}$ must be HIGH, the outputs must be enabled ($\overline{G}$ is LOW) and the addresses must be either stable or latched with ALE. Figure 12 is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both $\overline{S}_L$ and $\overline{S}_H$ are HIGH.

(2) $\overline{S}_H$ goes LOW initiating a Read on the upper byte $DQ_{H(9-17)}$. $\overline{S}_L$ remains HIGH keeping the lower byte $DQ_{L(0-8)}$ disabled and in a high-impedance mode.

(3) $\overline{S}_L$ goes LOW activating $DQ_{L(0-8)}$.Valid data is available in t_{SA} following $\overline{S}_L$ going LOW.

(4) When $\overline{S}_H$ goes HIGH, $DQ_{H(9-17)}$ remains valid for t_{SHZ} before returning to a high-impedance condition.

(5) Finally, the Read for the lower byte is terminated by deasserting $\overline{S}_L$ (HIGH). $DQ_{L(0-8)}$ remains active for t_{SHZ} following $\overline{S}_L$ going HIGH.

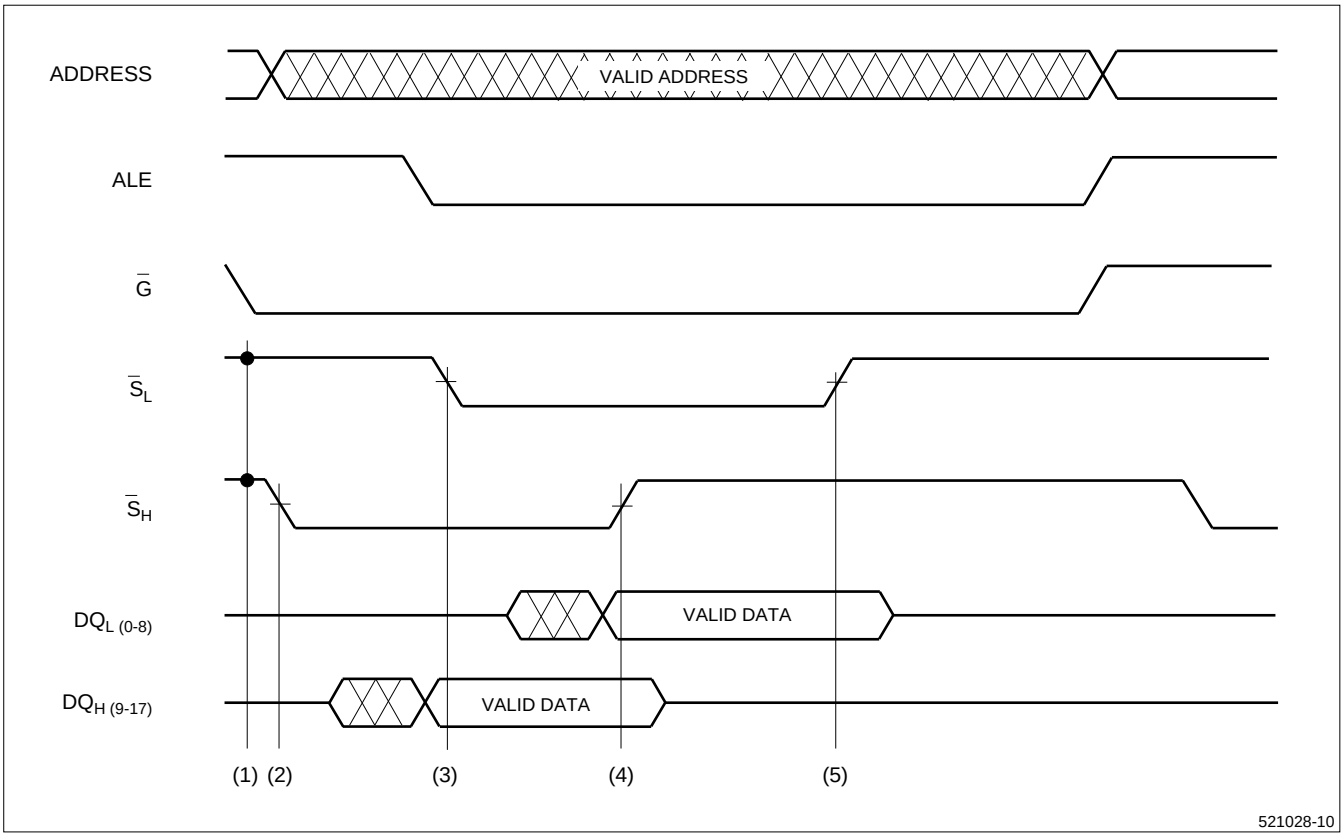


Figure 12. Byte Read ($\overline{E}$ is LOW and $\overline{W}$ is HIGH)

BYTE OPERATIONS (cont'd)

Byte Write Description (Figure 13)

To do individual byte-write operations, the device must be enabled ($\overline{E}$ is LOW, $\overline{G}$ is don't care) and addresses must be either stable or latched. Figure 13 is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

(1) $\overline{W}$ goes LOW while $\overline{S}_L$ and $\overline{S}_H$ remain HIGH.

(2) $\overline{S}_L$ goes LOW initiating a Write into the lower byte $DQ_{L(0-8)}$ of memory location N. $\overline{S}_H$ remains HIGH preventing a Write into the upper byte $DQ_{L(9-17)}$ of memory location N.

(3) $\overline{S}_L$ now goes HIGH terminating the Write operation on the lower byte of memory location N.

(4) Address N is changed to M.

(5) The Write operation is now initiated on the upper byte $DQ_{H(9-17)}$ by bringing $\overline{S}_H$ LOW. $\overline{S}_L$ remains HIGH preventing a Write operation from occurring in the lower byte $DQ_{L(0-8)}$ of memory location N+ 1.

(6) $\overline{S}_H$ now goes HIGH terminating the Write operation on the upper byte of address M.

(7) $\overline{W}$ goes HIGH, ending the Write operation.

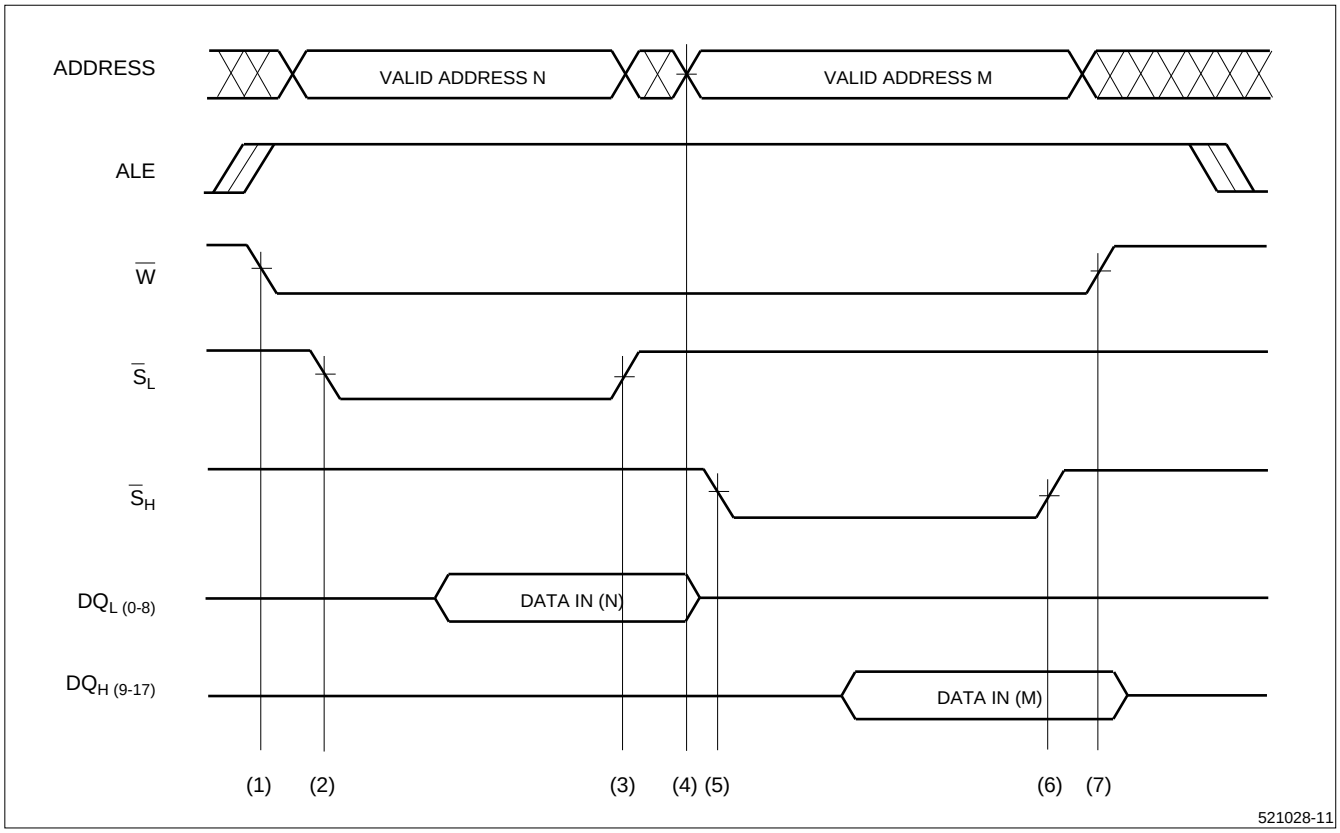
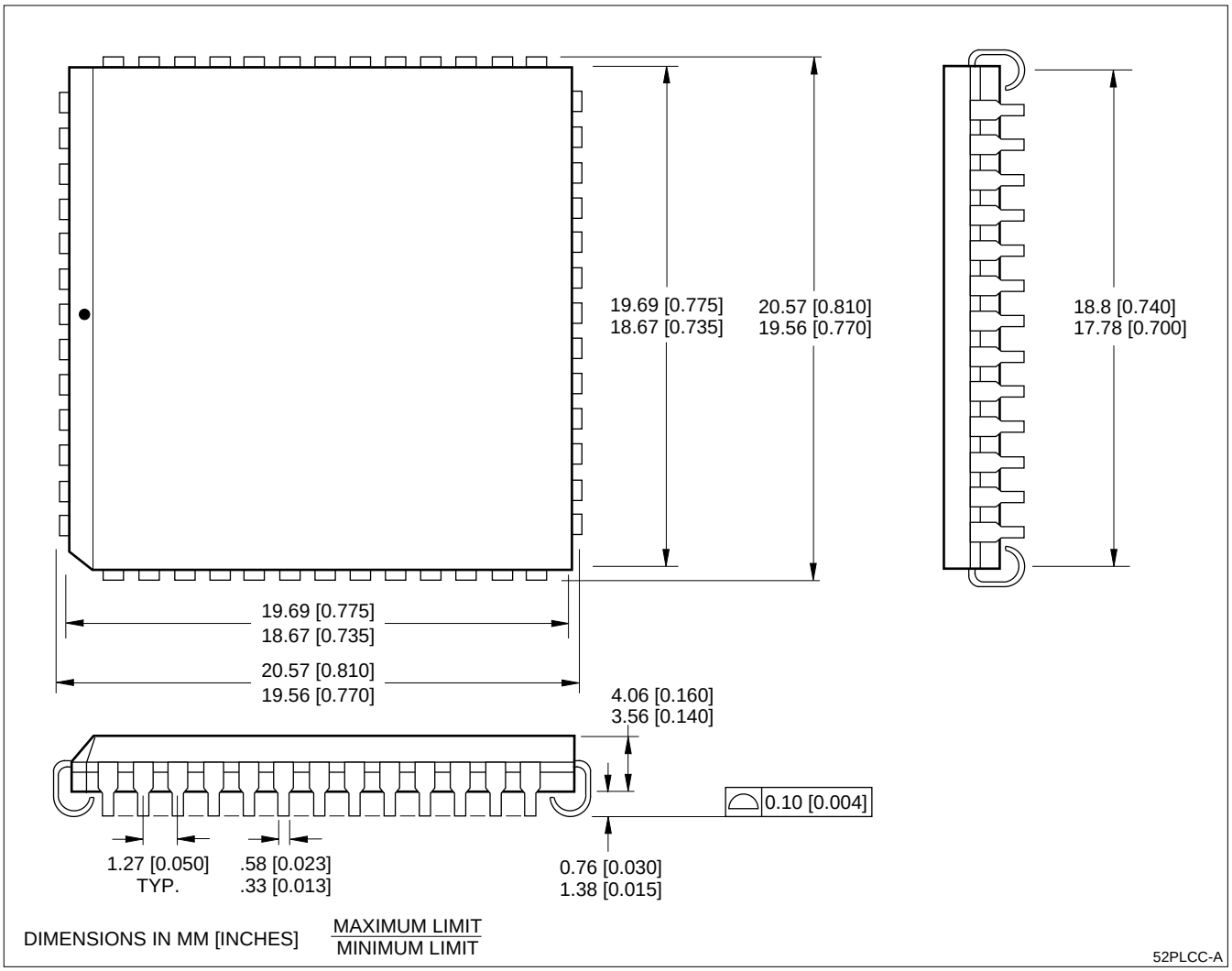


Figure 13. Byte Write ($\overline{E}$ is LOW)

PACKAGE DIAGRAM



52-Pin PLCC

ORDERING INFORMATION